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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/213,748	12/17/98	CALLWAY	E 0100.01319

EXAMINER	
HARRISON, C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/213,748	CALLWAY ET AL.	
	Examiner	Art Unit	
	Chante Harrison	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) 1 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 2-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto, U.S. Patent 5,912,710, 6/1999, 348/445.

As per independent claim 4, Fujimoto discloses a video scaler to receive and scale video based on a ratio between the input format and the output format (FIG. 1 "107"), a graphics scaler to receive and scale graphics based on a ratio between the input format and the output format (FIG. 1 "106"), combining the video and graphics to produce video graphics output (FIG. 1 "108"; FIG. 6; FIG. 8 "203"), a first memory (FIG. 8 "11") having graphics data and a second memory (FIG. 8 "13") having video data. Fujimoto fails to disclose the two memories coupled to their corresponding scalers. However it would have been obvious to one of skill in the art to use the disclosure of Fujimoto because he teaches storing the separate video and graphics data together on media accessible by the scaling and merging process.

As per dependent claims 2 and 21, Fujimoto discloses a controller (FIG. 8 "122") providing data to the video and graphics scalers (FIG. 8) and allocating memory to the

first and second blocks of memory, but fails to specifically disclose allocating memory based upon memory needs of the data stream. However it would have been obvious to one of skill in the art to use the disclosure of Fujimoto to allocate memory based on data needs because he teaches separately providing and scaling streams of data.

As per dependent claims 3 and 22, Fujimoto discloses the merging block receiving control data used to produce the video graphics output (FIG. 8 "201 & 203").

As per dependent claim 5, Fujimoto fails to disclose the first and second memory blocks included in a frame buffer of a video graphics integrated circuit. However it would have been obvious to use his disclosure because he teaches providing the data together on media accessible by the scaling and merging process (FIGS. 1 & 9).

As per dependent claim 6, Fujimoto discloses a video controller coupled to the video scaler (FIG. 1), a graphics controller coupled to the graphics scaler (FIG. 1) and the video and data controller are synchronized (FIG. 1; col. 10-11, ll. 60 et seq.).

As per dependent claim 7, Fujimoto discloses an alpha blend operation (FIG. 1 "108").

As per dependent claims 8 and 23, Fujimoto discloses a digital to analog converter for the video graphics (col. 10, ll. 35 et seq.).

As per dependent claim 9, Fujimoto discloses a display driver (FIG. 18 "18c") formatting the output (col. 6, ll. 40 et seq.; col. 10, ll. 10-25, 60 et seq.).

As per dependent claim 10, Fujimoto discloses a driver coupled to a video scaler (FIG. 18 "18c").

As per dependent claim 11, Fujimoto discloses a driver coupled to a graphics scaler (FIG. 18 "18c").

As per dependent claims 12 and 25, Fujimoto discloses a graphics flicker removal block (FIG. 16 "203"; col. 14, ll. 56 et seq.). It would have been obvious to one of skill to use the teachings of Fujimoto because he teaches a filter having a delay circuit (col. 16, ll. 56 et seq.) and selectable characteristics (col. 16, ll. 19 et seq.) and processing multiple scan lines, which implies an averaging technique (FIG. 11) that is known to reduce flicker.

As per dependent claims 13 and 24, Fujimoto discloses a video flicker removal block. The rejection as applied to claim 12 is included herein.

As per dependent claim 14, Fujimoto fails to disclose a plurality of graphics scalers. However it would have been obvious to use his disclosure because he teaches using a graphics scaler and supplying the scaled data in one of two formats.

As per dependent claim 15, Fujimoto discloses the merging block configuring a pixel rate of the video output stream to produce a preferred video scaling ratio (col. 2, ll. 46-64; col. 3, ll. 18-35).

As per dependent claim 16, Fujimoto discloses the merging block configuring a pixel rate of the video output stream to produce a preferred graphics scaling ratio (col. 2, ll. 46-64; col. 3, ll. 18-35).

As per dependent claims 17 and 28, Fujimoto discloses a video decompression block (FIG. 1 "102").

As per dependent claims 18 and 29, Fujimoto discloses a graphics decompression block (FIGS. 1 & 17; col. 15, ll. 10 et seq.).

As per dependent claim 19, Fujimoto discloses the video stream is a decoded MPEG data stream (FIG.1 "102").

As per independent claim 20, Fujimoto discloses allocating a first block of memory for storing the video data stream (FIG. 1 '100B'), allocating a second block of memory for storing the graphics data stream (FIG. 1 '100G'), a method (abstract) operable in the device of claim 1, but fails to specifically disclose allocating memory based upon memory needs of the data stream. However it would have been obvious to one of skill in the art to use the disclosure of Fujimoto to allocate memory based on data needs because he teaches separately providing and scaling streams of data. The rejection as applied to independent claim 1 is included herein.

As per dependent claim 26, Fujimoto discloses scaling the video based on a first format and a plurality of selected formats (FIG. 1 "107"; col. 6, ll. 45-48, 54-58).

As per dependent claim 27, Fujimoto discloses scaling the graphics based on a first format and a plurality of selected formats (FIG. 1 "106"; col. 6, ll. 45-48, 54-58).

As per independent claim 30, Fujimoto discloses a circuit (FIG.S. 1, 8 & 9) for implementing the method of claim 20. Therefore the rejection as applied to independent claim 20 is included herein.

As per independent claim 31, Fujimoto discloses plural memory blocks storing one of video and graphics data (FIG. 8), but fails to disclose a plurality of video scalers and graphics scalers that scales a portion of its respective data independent from the

other plurality of respective data streams and merging blocks. However it would have been obvious to one of ordinary skill in the art to use the disclosure of Fujimoto because he teaches dynamically changing control data (col. 16, ll. 19 et seq.) to provide a plurality of graphics and video data to independent graphics and video scalers to scale the respective data and merge the data to produce video graphics output in one of multiple selected display ratios.

As per dependent claim 32, Fujimoto discloses the video and graphics scalers and merging block in an integrated circuit (FIGS.1, 8 & 9), but fails to disclose a plurality of scalers and merging blocks. The rationale as applied to claim 31 is included herein.

As per dependent claim 33, Fujimoto discloses a portion of the memory blocks included in the circuit (FIG. 9).

As per dependent claim 34, Fujimoto discloses the controller coupled to the graphics and video scalers (FIG. 8), but fails to disclose multiple controllers. However it would have been obvious to one skilled in the art to use his disclosure because he teaches providing separate controlling data to each of a graphics and video scaler (col. 10-11, ll. 60 et seq.).

As per dependent claim 35, Fujimoto discloses the controller providing data to the merging block (FIG. 8 "201 & 203"), but fails to disclose a plurality of controllers and merging blocks. The rationale as applied to claim 31 is included herein.

As per dependent claim 36, Fujimoto discloses the merging block performing alpha blending (FIG. 1 "108"), but fails to disclose a plurality of merging blocks. The rationale as applied to claim 31 is included herein.

As per dependent claim 37, Fujimoto discloses the merging block producing video graphics output in one of an analog display format and a digital display format (col. 10, ll. 35 et seq.), but fails to disclose a plurality of merging blocks. The rationale as applied to claim 31 is included herein.

Response to Arguments

Applicant's arguments filed 6/25/01 have been fully considered but they are not persuasive. The claimed invention is obvious in view of Fujimoto because he discloses a system storing video and graphics data separately in a single memory, where the individual data is provided either selectively or at once to independent scalers that scale the respective data to one of a plurality of display ratios and merge the data to produce video graphics output (FIGS. 1, 6 &7). Therefore the rejection is maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Chante Harrison** whose telephone number is **(703) 305-3937**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Michael Razavi,** can be reached at **(703) 305-4713**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

MATTHEW LUU
PRIMARY EXAMINER